**Fig. 1A**

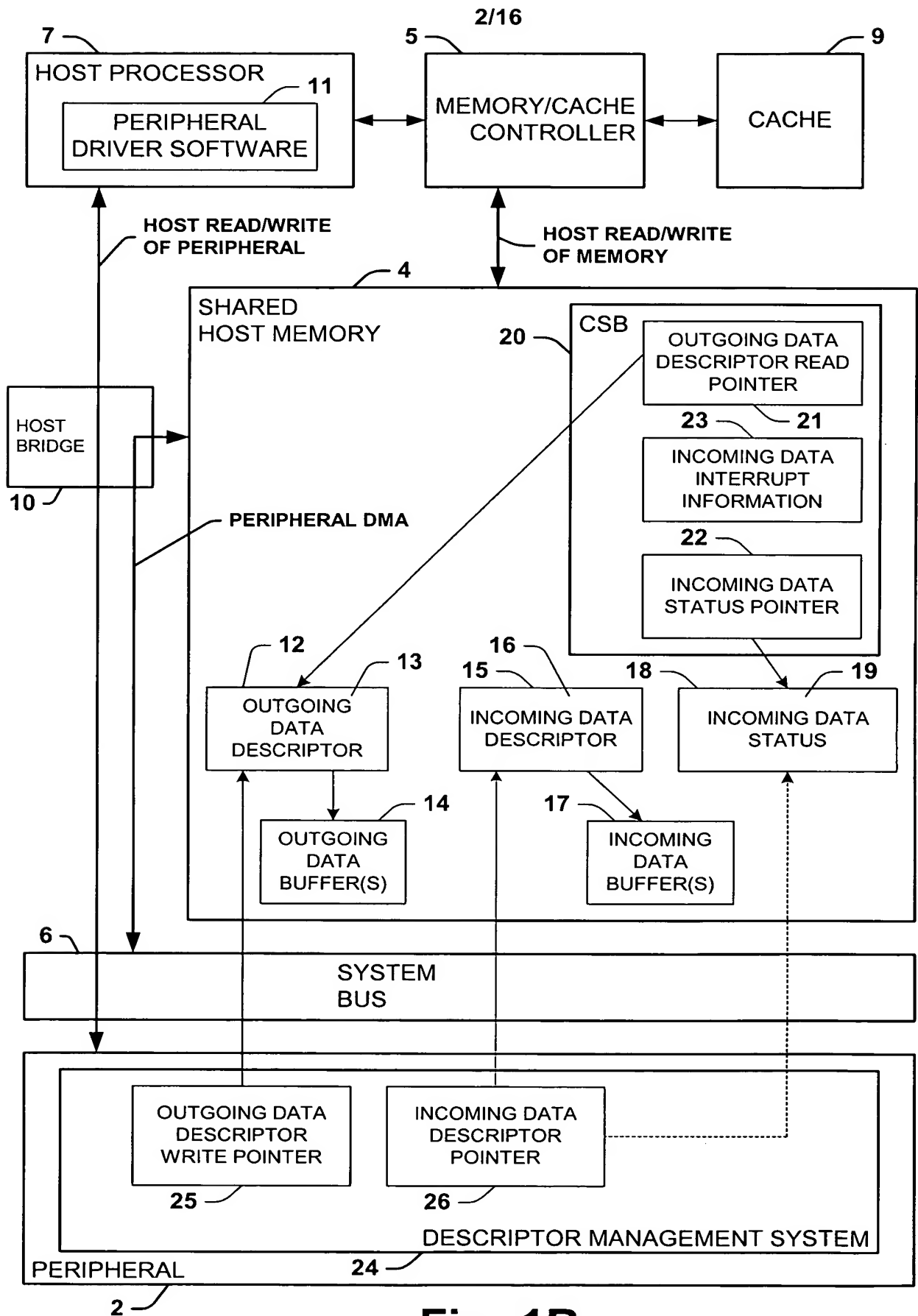
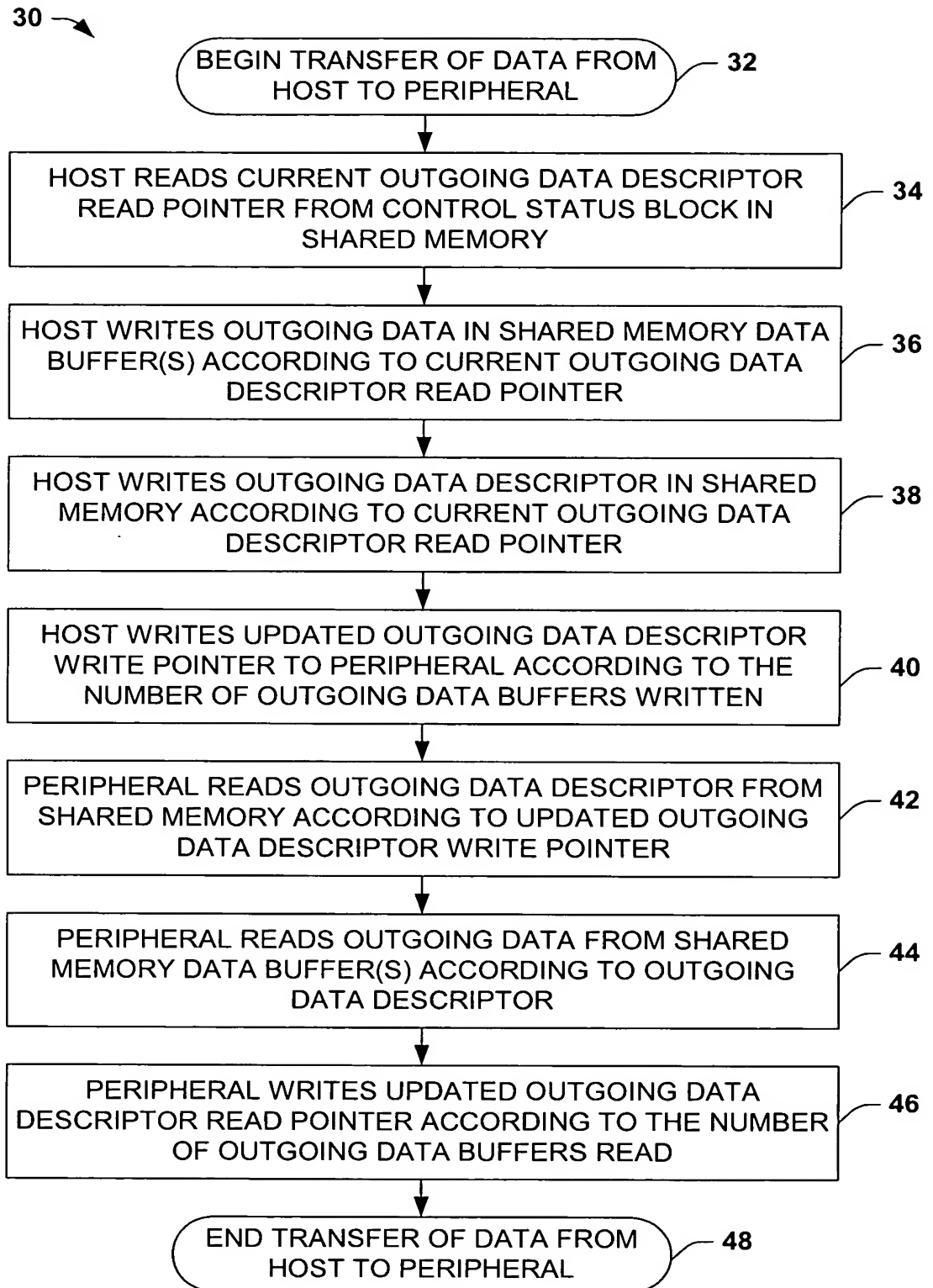
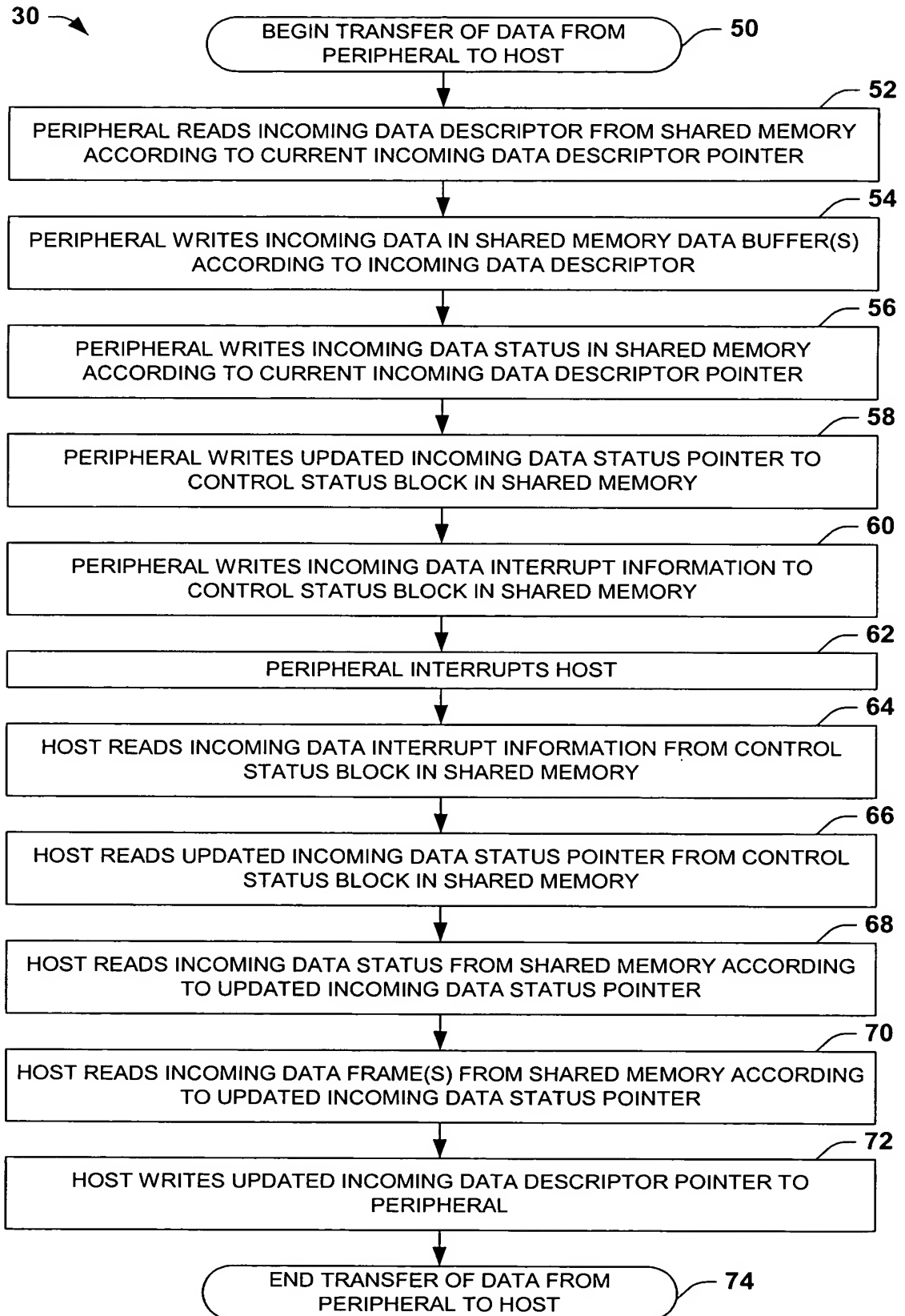


Fig. 1B

**Fig. 1C**

**Fig. 1D**

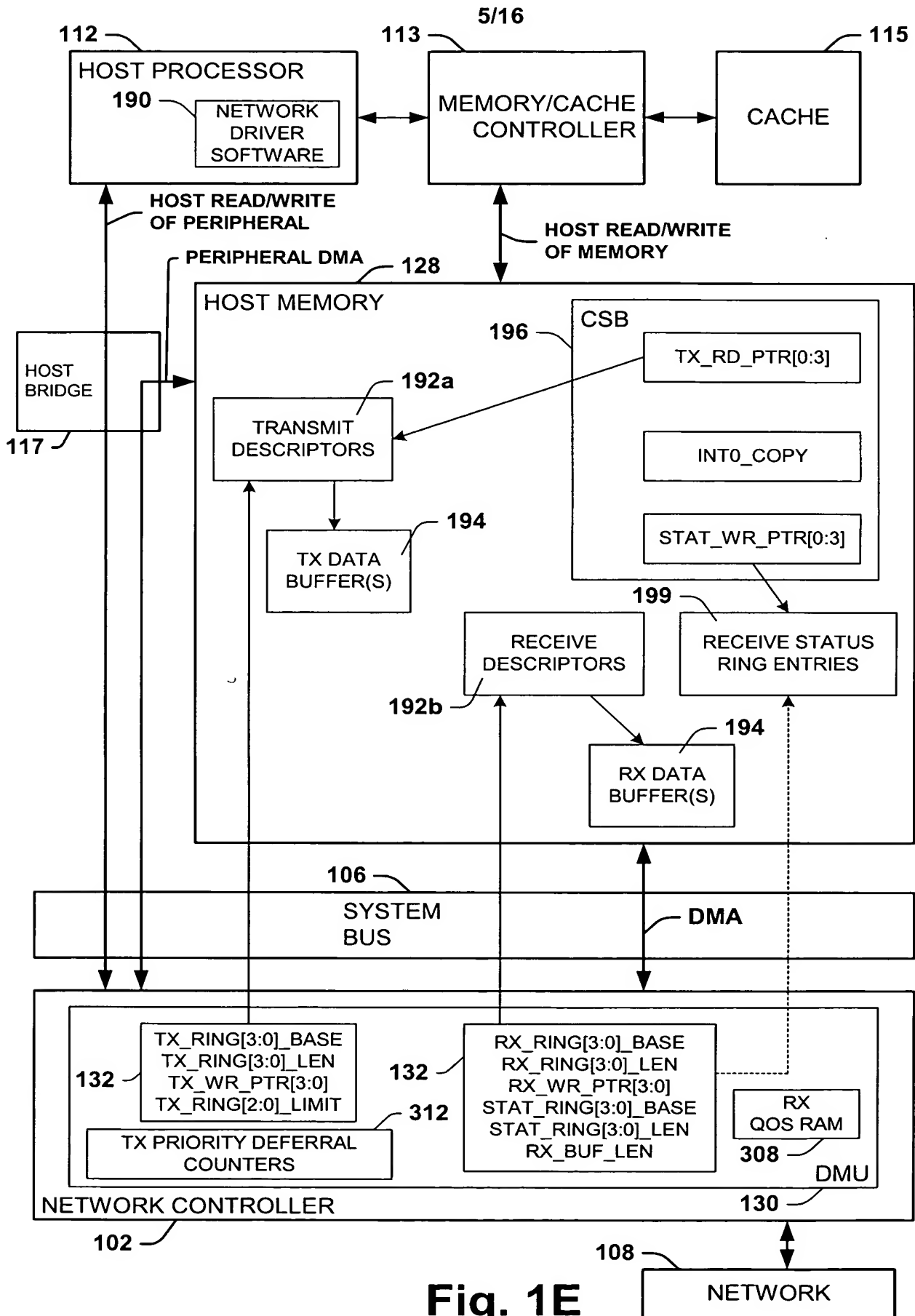


Fig. 1E

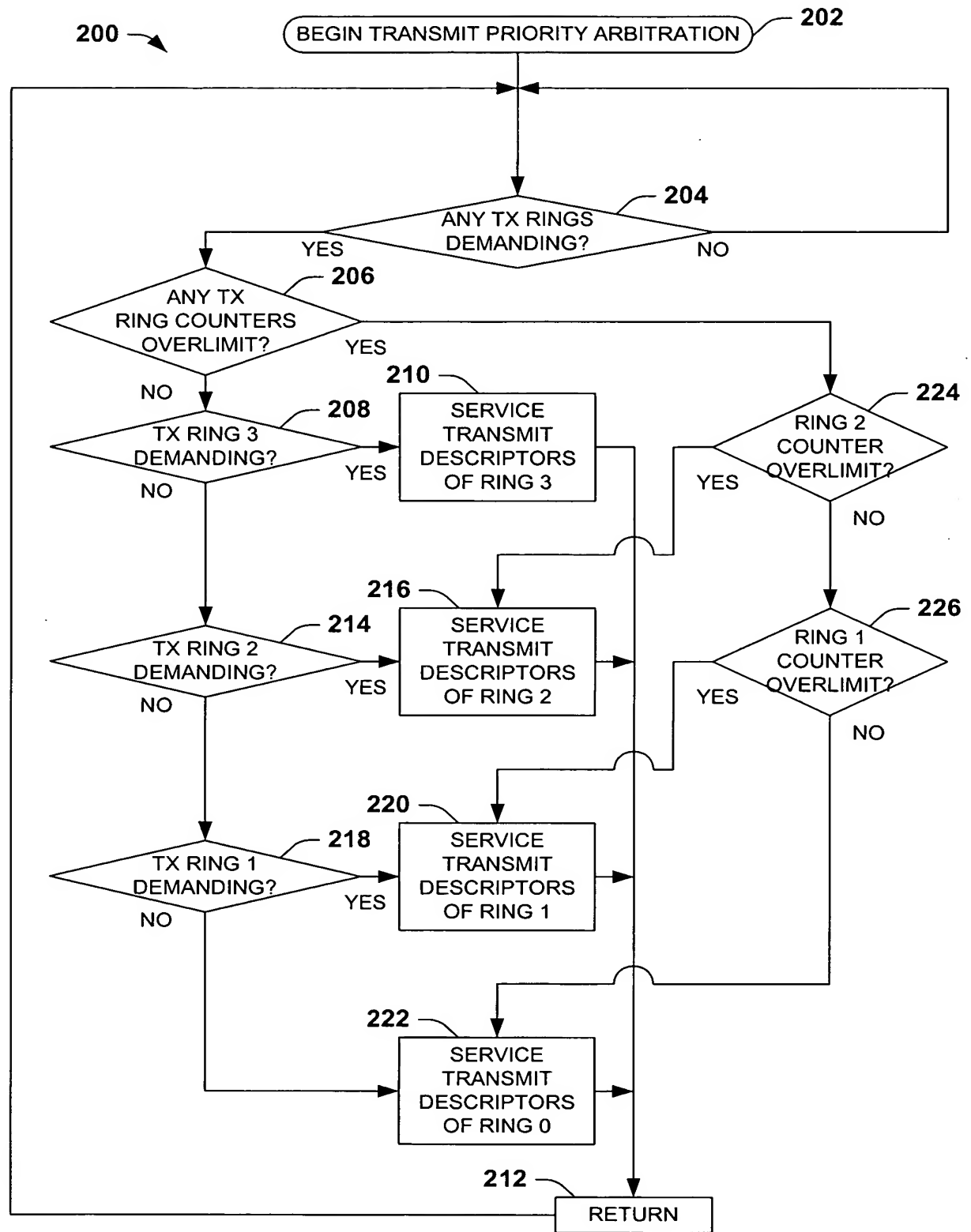


Fig. 1F

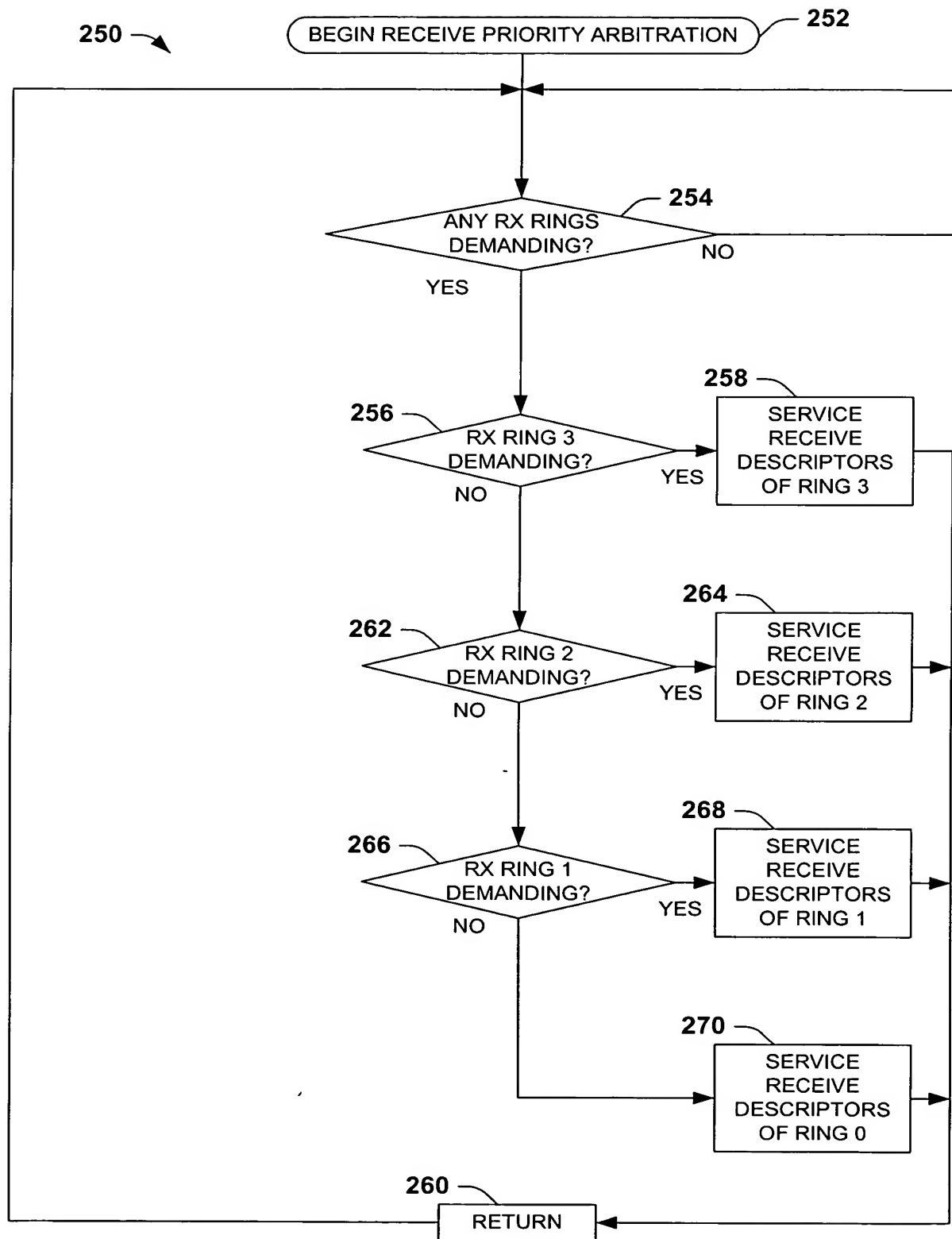


Fig. 1G

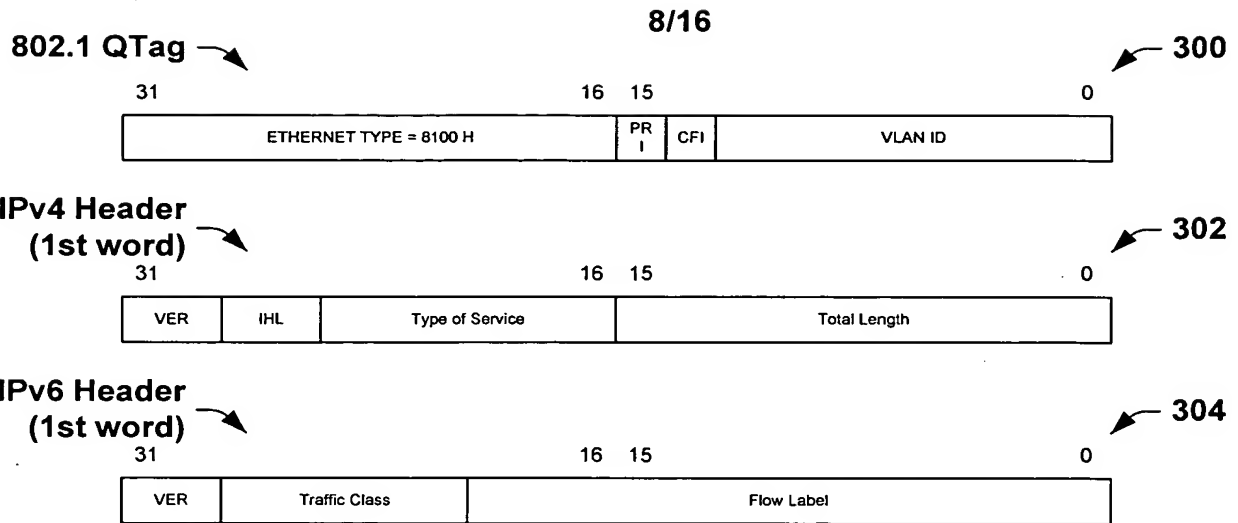


Fig. 1H

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PREF_QTAG	ALT_PRI_OK	QTAG EXISTS	IP HEADER EXISTS	PRIORITY SOURCE
1	X	YES	X	QTAG
1	0	NO	X	DEFAULT REGISTER
1	1	NO	YES	IP HEADER
X	X	NO	NO	DEFAULT REGISTER
0	X	X	YES	IP HEADER
0	0	X	NO	DEFAULT REGISTER
0	1	YES	NO	QTAG

Fig. 1I

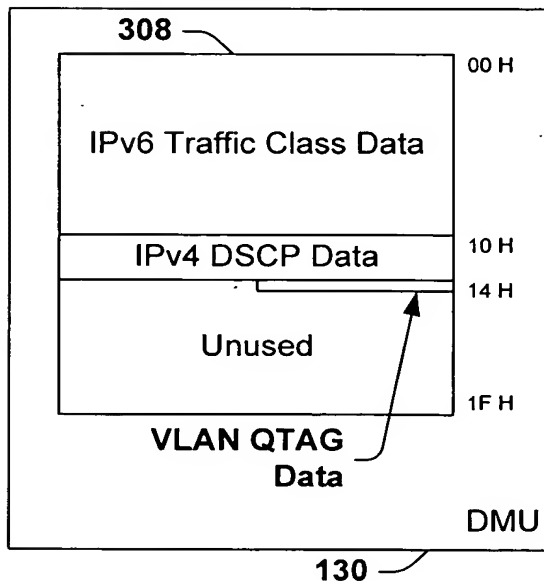


Fig. 1J

PRIORITY SOURCE	VALUE	RAM ADDRESS	BITS
Traffic Class	00 H	00 H	1:0
Traffic Class	0F H	00 H	31:30
Traffic Class	10 H	01 H	1:0
Traffic Class	F0 H	0F H	1:0
DSCP	30 H	13 H	1:0
DSCP	3F H	13 H	31:30
QTAG PRIORITY	0	14 H	1:0
QTAG PRIORITY	7	14 H	15:14

Fig. 1K

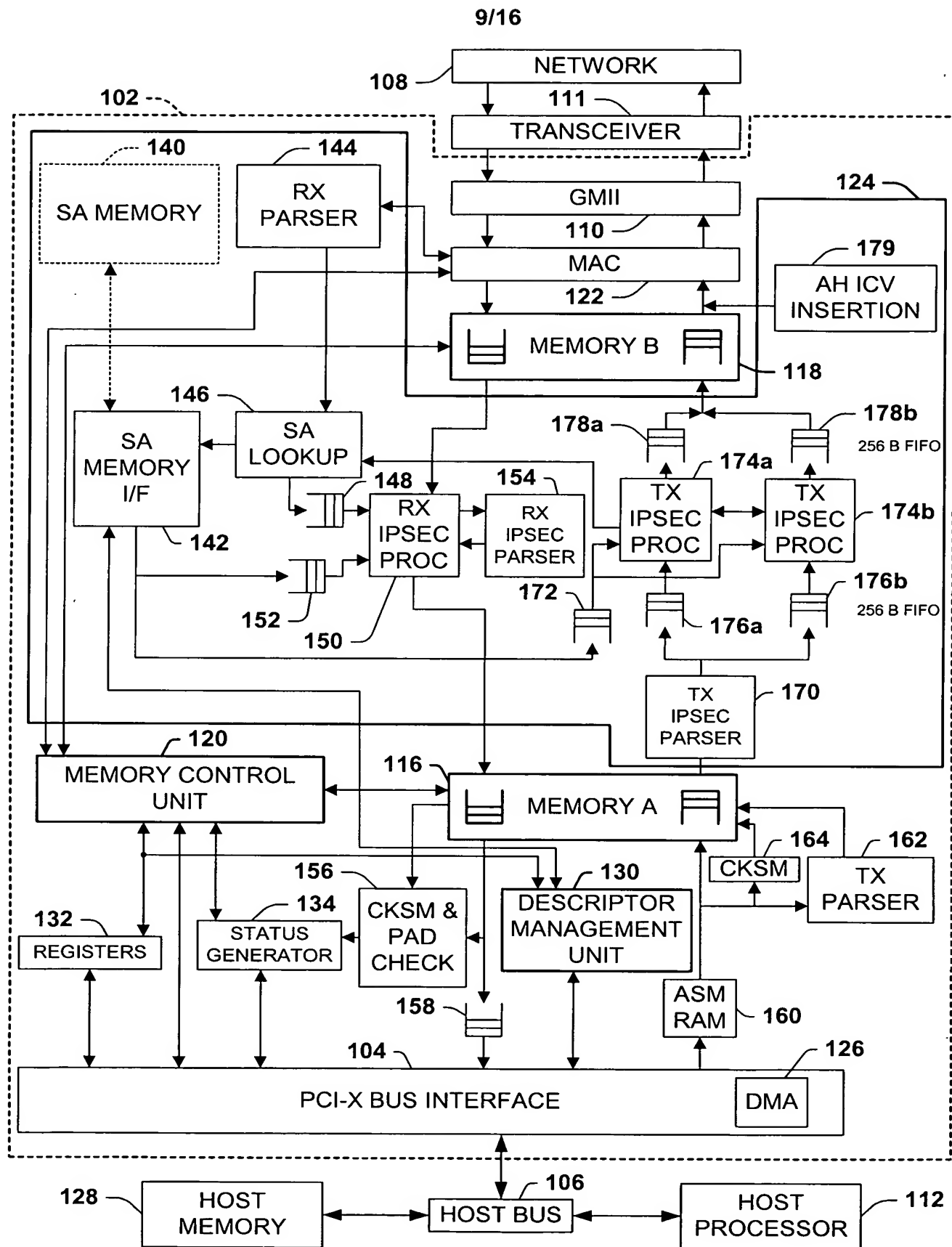


Fig. 2

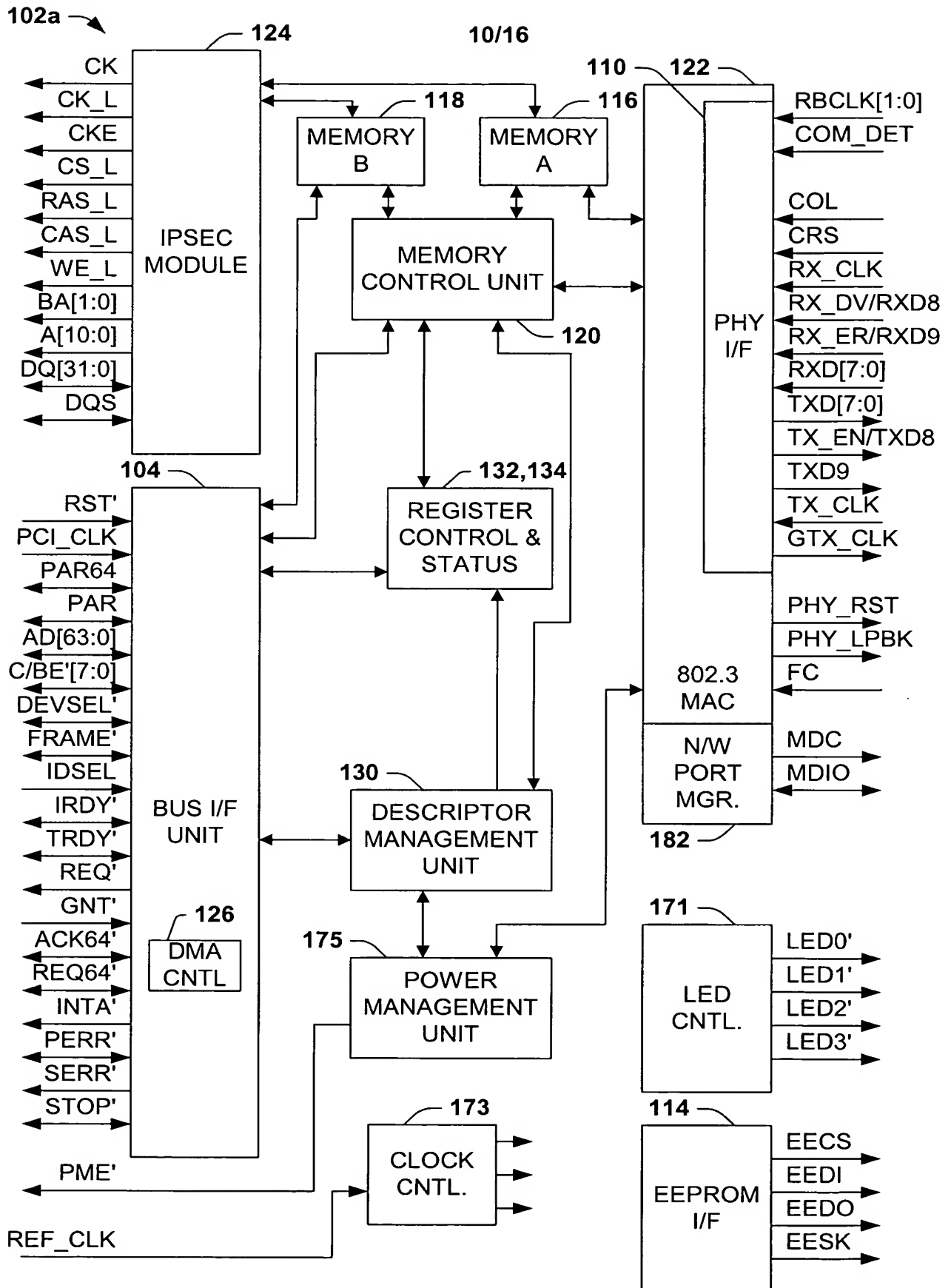
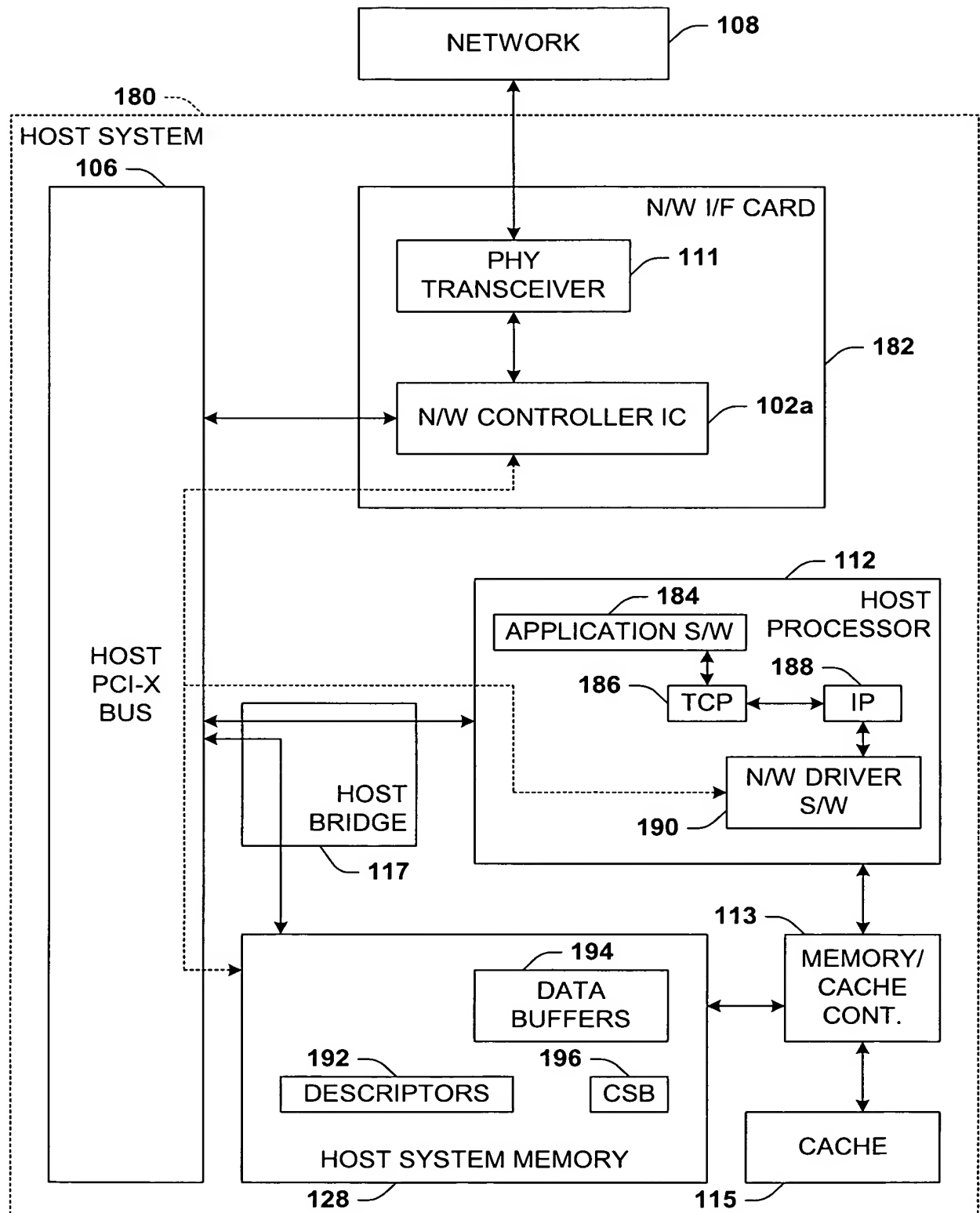


Fig. 3

**Fig. 4**

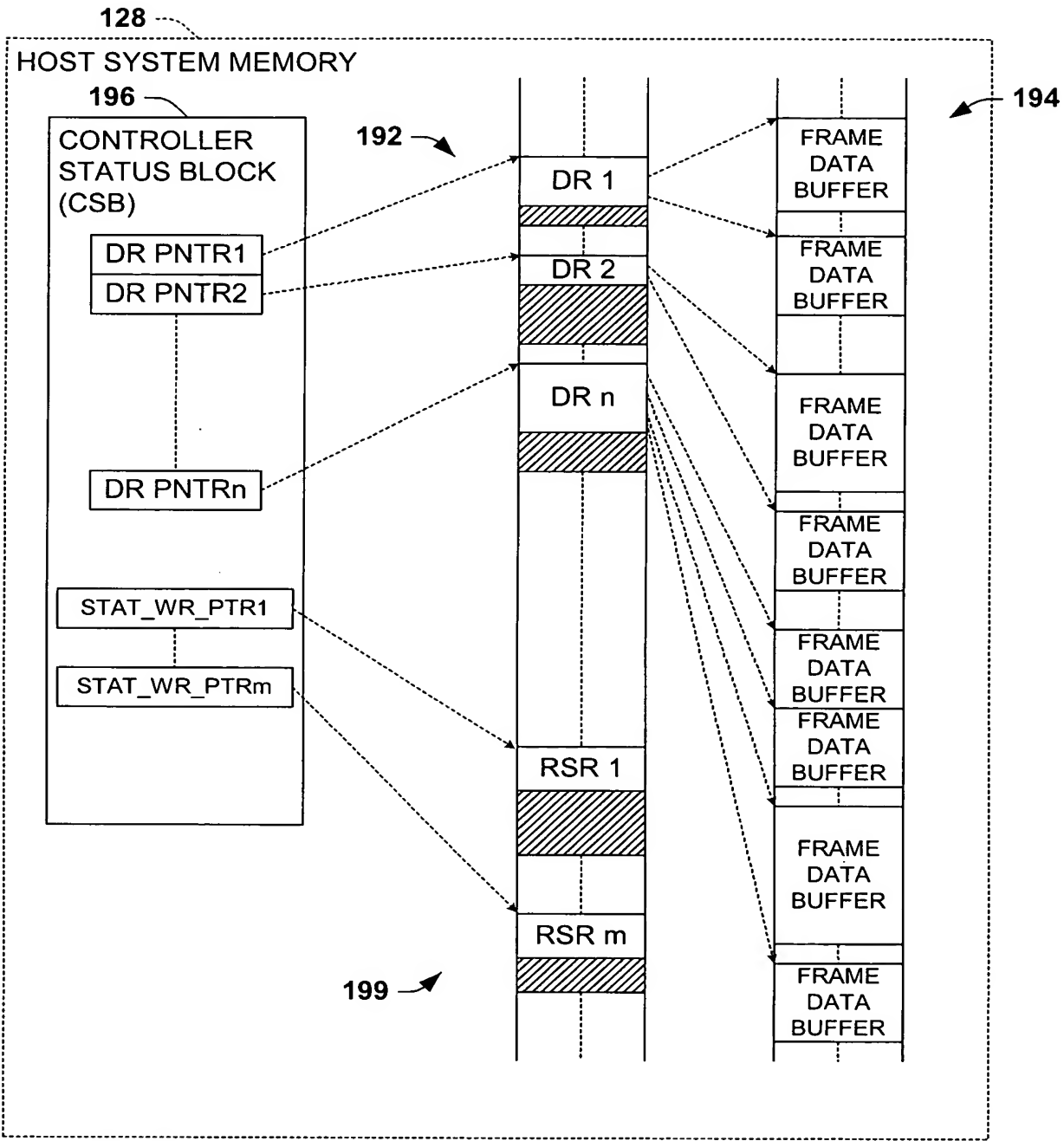


Fig. 5A

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CSB

TX_RD_PTR0
TX_RD_PTR1
TX_RD_PTR2
TX_RD_PTR3
STAT_WR_PTR0
STAT_WR_PTR1
STAT_WR_PTR2
STAT_WR_PTR3
INT0_COPY

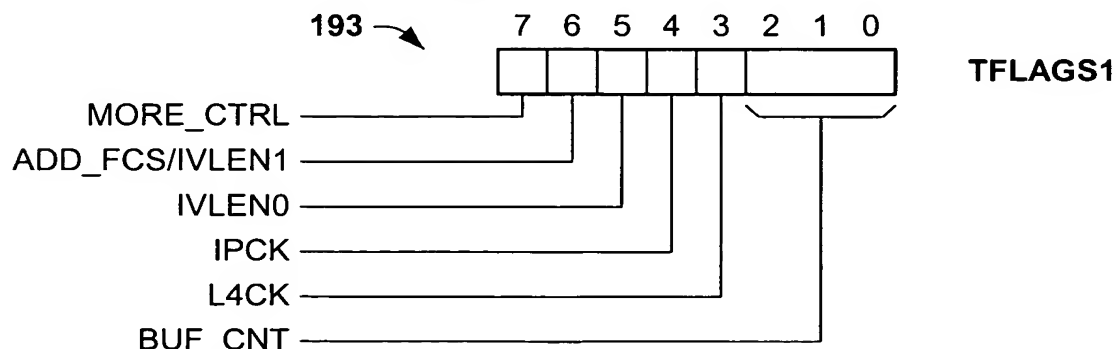
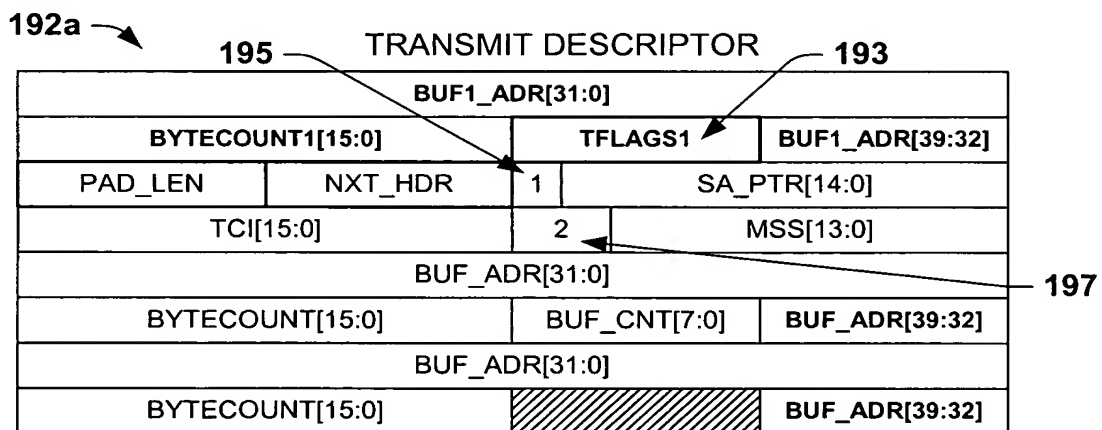
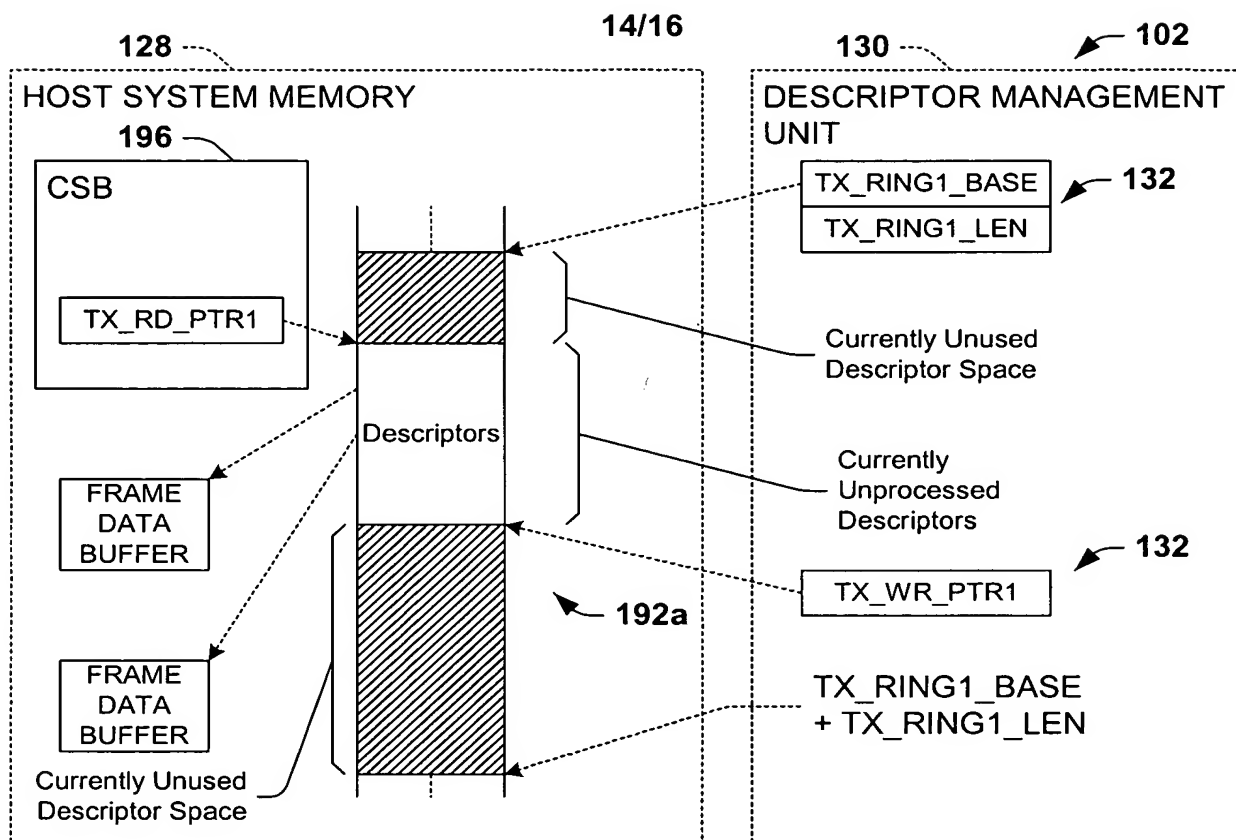
Fig. 5B

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REGISTERS

RX_RING[3:0]_BASE
TX_RING[3:0]_BASE
RX_RING[3:0]_LEN
TX_RING[3:0]_LEN
TX_WR_PTR[3:0]
RX_WR_PTR[3:0]
STAT_RING[3:0]_BASE
STAT_RING[3:0]_LEN
RX_BUF_LEN
CSB_ADDR

Fig. 5C



192b →

RECEIVE DESCRIPTOR

BUF_ADR[31:0]		
RES	BUF_MULT[7:0]	BUF_ADR[39:32]

Fig. 5G

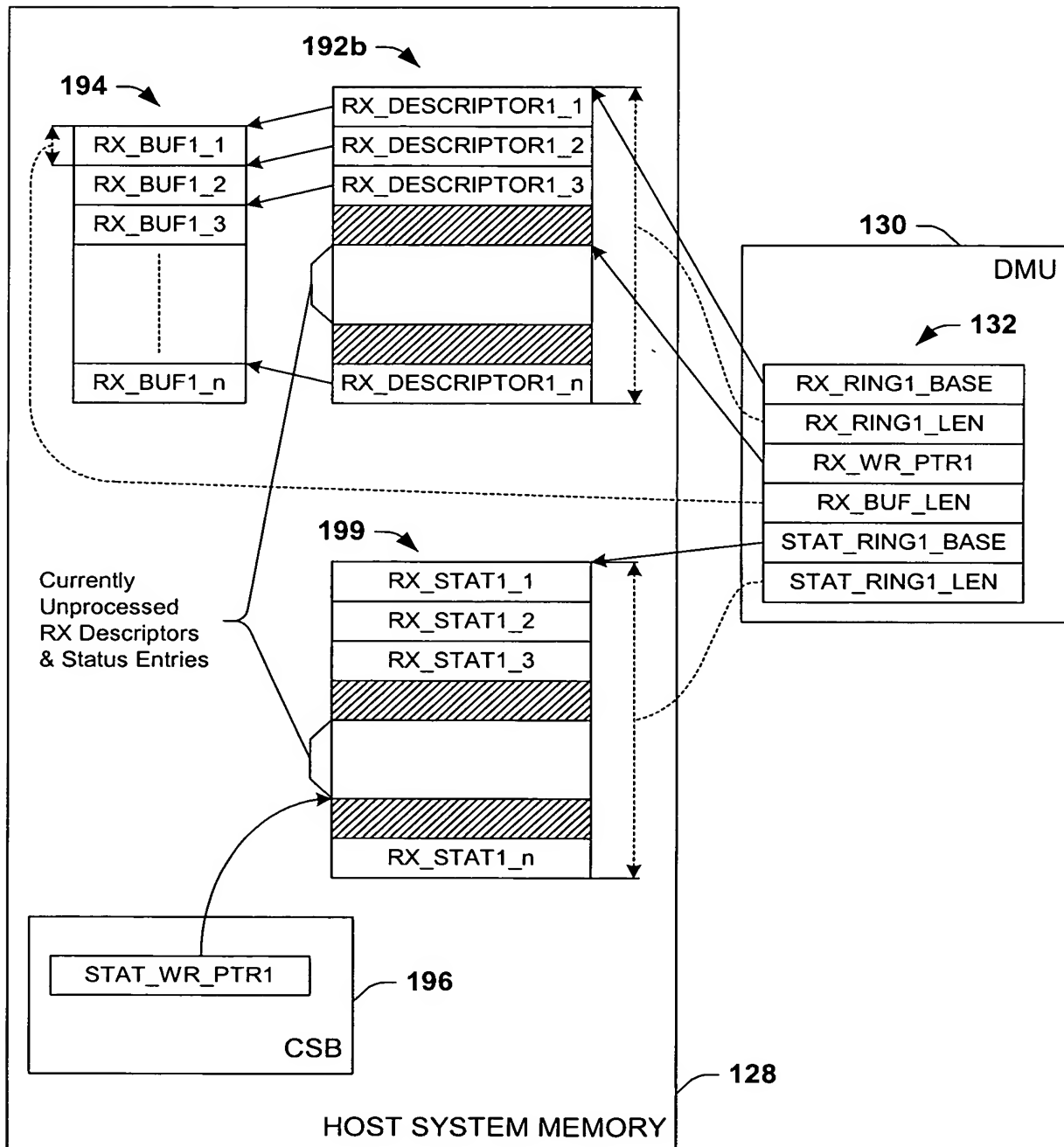


Fig. 5H

